CLAIMS

1. A pulse-width modulation (PWM) system that minimizes output ripple of a multiphase DC-DC converter which converts N input voltages including at least one dissimilar input voltage, said PWM system comprising:

   PWM waveform logic that generates N PWM signals including a PWM signal for each of the N input voltages; and

   PWM control logic that optimizes relative phases of said N PWM signals based on voltage levels of the N input voltages.

2. The PWM system of claim 1, wherein said PWM control logic centers pulses of said N PWM signals for each PWM cycle.

3. The PWM system of claim 1, wherein said PWM control logic distributes pulses of said N PWM signals based on predetermined phase angles including at least one phase angle other than 360/N degrees.

4. The PWM system of claim 1, wherein said PWM control logic includes conversion logic that determines input voltage levels and select logic that selects at least one of a plurality of predetermined phase angles.

5. The PWM system of claim 4, wherein said conversion logic comprises an analog to digital converter that determines said input voltage levels from among a plurality of predetermined voltage levels and wherein said select logic comprises a lookup table that stores a plurality of predetermined phase values.

6. The PWM system of claim 4, wherein said conversion logic determines said input voltage levels from a plurality of predetermined voltage levels, digital logic that generates a plurality of phase signals each having a phase angle associated with a combination of said plurality of predetermined voltage levels, and phase select logic that selects from among said plurality of phase signals.

7. The PWM system of claim 6, wherein said conversion logic comprises an analog to digital converter that generates digital values, and wherein said phase select logic comprises a decoder that converts said digital values to corresponding select signals and a multiplexer that selects from among said phase signals based on said select signals.

8. The PWM system of claim 1, wherein said PWM control logic includes conversion logic that measures input voltage levels and computation logic that calculates at least one optimal phase angle based on measured input voltage levels.

9. The PWM system of claim 1, wherein N = 2, wherein said PWM waveform logic generates first and second PWM signals, and wherein said PWM control logic comprises:

detection logic that measures a first delay from termination of each pulse of said first PWM signal and initiation of a next pulse of said second PWM signal and a second delay from termination of each pulse of said second PWM signal and initiation of a next pulse of said first PWM signal; and

phase-locked loop logic that adjusts phase of said second PWM signal to equalize said first and second delays.

10. The PWM system of claim 1, wherein said PWM control logic comprises phase-locked loop logic that measures and equalizes off-times between consecutive pulses of said N PWM signals.

11. A DC-DC converter, comprising:

a plurality of channels, each receiving a corresponding one of a plurality of input voltages including at least one dissimilar input voltage, and developing an output voltage using a corresponding one of a plurality of PWM signals; and

PWM logic that generates said plurality of PWM signals with optimized phase angles to minimize output ripple.

12. The DC-DC converter of claim 11, wherein said PWM logic equalizes off-times between consecutive pulses of said plurality of PWM signals.

13. The DC-DC converter of claim 12, wherein said PWM logic comprises phase-locked loop logic that measures and equalizes off-times between consecutive pulses of said plurality of PWM signals.

14. The DC-DC converter of claim 11, wherein said plurality of PWM signals includes first and second PWM signals with unequal pulse widths, and wherein said PWM logic shifts said second PWM signal relative to said first PWM signal by a predetermined phase angle.

15. The DC-DC converter of claim 11, wherein said PWM logic includes conversion logic that determines input voltage levels and select logic that determines at least one corresponding phase angle.

16. The DC-DC converter of claim 15, wherein said conversion logic selects from among a plurality of predetermined input voltage levels and wherein said select logic comprises a memory with pre-stored phase values.

17. The DC-DC converter of claim 15, wherein said conversion logic comprises an analog to digital converter that measures said input voltage levels and wherein said select logic comprises computation logic that calculates at least one optimal phase angle based on measured input voltage levels.

18. The DC-DC converter of claim 15, further comprising:

said conversion logic selecting from among a plurality of predetermined input voltage levels;

digital logic that generates a plurality of phase signals based on a master clock signal and associated with combinations of said predetermined input voltage levels; and

said select logic selecting from among said plurality of phase signals.

19. The DC-DC converter of claim 18, wherein said conversion logic comprises an analog to digital converter that generates digital voltage signals, and wherein said select logic comprises a decoder that converts said digital voltage signals to corresponding select signals a multiplexer that selects from among said phase signals based on said select signals.

20. The DC-DC converter of claim 11, wherein said plurality of PWM signals includes first and second PWM signals with unequal pulse widths, and wherein said PWM logic comprises:

detection logic that measures a first delay from termination of each pulse of said first PWM signal and initiation of a next pulse of said second PWM signal and a second delay from termination of each pulse of said second PWM signal and initiation of a next pulse of said first PWM signal; and

phase-locked loop logic that adjusts phase of said second PWM signal to equalize said first and second delays.

21. A method of reducing ripple of a multiphase DC-DC converter that converts N input voltages including at least one dissimilar input voltage, comprising:

generating N pulse-width modulated (PWM) waveforms each corresponding to one of the N input voltages; and

adjusting phase of at least one of the PWM waveforms to achieve an optimal phase relationship in which at least one pulse is initiated at a phase angle other than 360/N degrees during each PWM cycle.

22. The method of claim 21, wherein said adjusting phase comprises centering PWM pulses relative to each other.

23. The method of claim 21, further comprising measuring off-times between consecutive PWM pulses and wherein said adjusting comprises equalizing measured off-times.

24. The method of claim 23, wherein said measuring and equalizing comprises employing a phase-locked loop circuit.

25. The method of claim 21, further comprising:

determining input voltage levels;

determining at least one optimal phase angle based on determined input voltage levels; and

wherein said adjusting phase comprises adjusting phase of at least one PWM waveform based on the at least one optimal phase angle.

26. The method of claim 25, wherein said determining input voltage levels comprises selecting from among a plurality of predetermined voltage levels.

27. The method of claim 26, wherein said determining at least one optimal phase angle comprises reading a phase value from a memory device.

28. The method of claim 26, further comprising generating a plurality of phase signals and wherein said determining at least one optimal phase angle comprises selecting a phase signal based on selected voltage levels.

29. The method of claim 28, wherein said generating a plurality of phase signals comprises dividing a master clock signal by a sufficient number to provide an optimal phase relationship for each expected combination of input voltage levels.

30. The method of claim 25, wherein:

said determining input voltage levels comprises measuring input voltage levels; and

wherein said determining at least one optimal phase angle comprises calculating at least one optimal phase value based on measured input voltage levels.